Claims

[c1] What is claimed is:

1.A data recovery method for recovering digital data from a corresponding input signal, the digital data being synchronized with a data clock, the data clock comprising a plurality of data periods, amplitude of the input signal during each data period of the data clock representing the digital data;

the data recovery method comprising:

selecting a sampling clock with a predetermined sampling frequency, the sampling clock comprising a plurality of sampling periods;

calculating at least a control word during each sampling period, each control word being used for estimating a phase error between the sampling period and the corresponding data period;

calculating an original amplitude of said input signal within each data period of the data clock according to the corresponding control word and amplitude of said input signal during each sampling period of the sampling clock for recovering the digital data; and

storing said original amplitude of said input signal of the corresponding control word;

wherein the sampling frequency, in a frequency domain, is higher than a maximum frequency of the input signal bandwidth and is lower than a frequency of the data clock.

[c2] 2. The data recovery method of claim 1 wherein said control word is calculated according to the amplitude of said input signal during the corresponding sampling period.

[c3] 3. The data recovery method of claim 1 wherein the input signal is outputted from an optical disk storage device, such as a compact disk (CD) player, CD-ROM or digital versatile disc (DVD) device.

[c4] 4. The data recovery method of claim 1 further comprising the step of using the recovered digital data to adjust the control word further.

[c5] 5. The data recovery method of claim 1 wherein a weighted interpolation algorithm is used for calculating the original amplitude of the input signal

during each data period according to the corresponding control words and amplitude of the input signal during each sampling period.

[c6] 6. A data recovery circuit for recovering digital data from a corresponding input signal, the digital data being synchronized with a data clock, the data clock comprising a plurality of data periods, amplitude of the input signal during each data period of the data clock representing the digital data;
the data recovery circuit comprising:
a sampler for measuring amplitude of said input signal during each sampling period, a duration of each sampling period being fixed and being related to a sampling frequency;
a computation module for calculating at least a control word during each sampling period, each control word being used for estimating a phase error between said sampling period and the corresponding data period; and
at least an interpolator, each interpolator respectively handling each control word during one sampling period for calculating each amplitude of said input signal during each data period according to both the corresponding control word and an output of the sampler in order to recover said digital data;
wherein said sampling frequency, in a frequency domain, is higher than a maximum frequency of the input signal bandwidth and is lower than a frequency of said data clock.

[c7] 7. The data recovery circuit of claim 6 further comprises a storage medium connected to said interpolator to receive said amplitude of said input signal within each of said data clock period and to generate the recovered digital data.

[c8] 8. The data recovery circuit of claim 6 wherein the control word is calculated according to the amplitude of said input signal during the corresponding sampling period.

[c9] 9. The data recovery circuit of claim 6 wherein the computation module uses the recovered digital data to adjust the control word further.

[c10] 10. The data recovery circuit of claim 6 wherein said interpolator uses a weighted interpolation algorithm for calculating the original amplitude of the

input signal during each data period according to the corresponding control words and amplitude of the input signal during each sampling period.

[c11] 11. A data recovery circuit for recovering digital data with a relative low sampling frequency, the data recovery circuit comprising:
a sampling device for sampling an analog input signal to generate a sequence of discrete time sample values that represent amplitudes of said input signal during each sampling period, a duration of each sampling period being fixed and being inversely related to said sampling frequency;
a computation module responsive to an output signal for calculating a plurality of control words during each sampling period, said control words being used for estimating a phase error between said sampling period and a data clock period; and
a plurality of interpolators, each interpolatorrespectively handling each of said control words during one sampling period together with each of said discrete time sample values for calculating an amplitude of said input signal within each of said data clock period in order to recover said digital data.

[c12] 12. The data recovery circuit of claim 11 further comprises a storage medium connected to said plurality of interpolators to receive said amplitude of said input signal within each of said data clock period and to generate said output signal.

[c13] 13. The data recovery circuit of claim 11 wherein said computation module comprises a plurality of computation units for generating said plurality of control words.

[c14] 14. The data recovery circuit of claim 11 wherein said sampling frequency, in a frequency domain, is higher than a maximum frequency of the input signal bandwidth and is lower than a frequency of said data clock.

[c15] 15. The data recovery circuit of claim 11 wherein said control word is calculated according to the amplitude of said input signal during the corresponding sampling period.

[c16] 16. The data recovery circuit of claim 11 wherein said interpolator uses a

weighted interpolation algorithm for calculating the original amplitude of said input signal during each data period according to the corresponding control word and amplitude of the input signal during each sampling period.

[c17] 17. A data recovery circuit for recovering digital data with a relative low sampling frequency, the data recovery circuit comprising:
a sampling device for sampling an analog input signal to generate a sequence of discrete time sample values that represent amplitudes of said input signal during each sampling period, a duration of each sampling period being fixed and being inversely related to said sampling frequency;
a computation module responsive to a recovered digital data for calculating a plurality of control words during each sampling period, said control words being used for estimating a phase error between said sampling period and a data clock period;
a plurality of interpolators, each interpolator respectively handling each of said control words during one sampling period together with each of said discrete time sample values for calculating an amplitude of said input signal within each of said data clock period in order to recover said digital data; and
a data buffer connected to said plurality of interpolators to receive said amplitude of said input signal within each of said data clock period and to generate said recovered digital data;
wherein said sampling frequency, in a frequency domain, is higher than a maximum frequency of the input signal bandwidth and is lower than a frequency of said data clock.

[c18] 18. The data recovery circuit of claim 17 wherein said computation module comprises a plurality of computation units for generating said plurality of control words.

[c19] 19. The data recovery circuit of claim 17 wherein said control word is calculated according to the amplitude of said input signal during the corresponding sampling period.

[c20] 20. The data recovery circuit of claim 17 wherein said interpolator uses a weighted interpolation algorithm for calculating the original amplitude of said

input signal during each data period according to the corresponding control word and amplitude of the input signal during each sampling period.